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# LSI Transceiver Chips Complete GPIB Interface

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# LSI TRANSCEIVER CHIPS COMPLETE GPIB INTERFACE

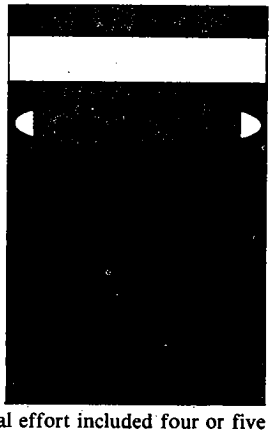
## A GPIB interface meeting IEEE 488 standards can be built with only three or four chips!

**by Pradip Madan and Jim Frederick**

The decision to support the IEEE 488 standard with integrated circuits was based on the potential popularity of the interface standard and its applications potential. Although a serial interface supports many system throughput requirements, a parallel interface over short distances can provide much higher data transfer rates, yet remain economical despite the extra interconnection copper required.

The IEEE 488 standard is for a parallel interface designed to operate over a limited distance. Its general purpose nature makes the general purpose interface bus (GPIB) attractive for a variety of systems, and also allows manufacturers to design their equipment interfaces to a common standard. As a result, users can mix equipment from different manufacturers without having to adapt the interfaces for compatibility. To date the GPIB has been incorporated in computer peripherals, such as printers, but the most applications have been in programmable instrumentation systems. Other GPIB applications include camera control in computer controlled studios, electronic surveillance, peripheral control, modular add-ons to photocopiers, and so forth.

### Integration benefit



Shortly after the IEEE committee had put the final touches on its standard specifications, engineers began building GPIB interface subsystems. Because the standard had just been defined, there were no large scale integration (LSI) chips available. Therefore, the first GPIB implementations were board level designs replete with small scale integration (SSI) and medium scale integration (MSI) logic chips. A typical effort included four or five rows of ten chips each.

With the advent of integrated circuit GPIB chips, chip counts dropped dramatically, reliability improved, and space requirements shrank. Consequently, the price range of systems for which GPIB had become practical began to decrease. A fully functional GPIB subsystem can now be constructed with less than one-tenth the number of chips formerly required. In fact, the complete

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talker/listener/controller mode logic resides in four LSI chips: one Intel 8291A talker/listener, one 8292 controller, and two 8293 transceivers. All these LSI, including the transceiver, are implemented in metal oxide semiconductor (MOS) technology.

Unlike the controller or talker/listener functions which could be integrated routinely in N-channel MOS (NMOS) technology, the transceiver posed special problems in MOS integration.

*The chip's size includes a 7-mil ground line and two ground pads in order to handle the 432-mA current.*

The standard calls for the transceiver circuitry to be able to drive each of the 16 bus lines with a nominal 48 mA of current. In addition, it specifies a minimum required input hysteresis and places a limit on propagation delays. Driving relatively high currents quickly was not a familiar province of MOS technology. Certainly the garden variety NMOS lacked the necessary speed-power product to handle the task.

However, progress in NMOS technology has produced the high speed, densely integrated high performance MOS (HMOS) technology which has the necessary characteristics to meet the current drive and propagation speed requisites.

### Designing the 8293 transceiver

Although the 48-mA drive required by the 16 GPIB lines had only been implemented with bipolar technology before, HMOS technology—with its reduced gate lengths, smaller size, and lower parasitic capacitance—looked like it could handle the job. Architecturally, the 8293 contains nine transceiver circuits which can be configured for data or interface management line transceivers. Nine open collector or 3-state line drivers that could sink 48 mA, in addition to twelve Schmitt-type line receivers, were used to implement the nine transceivers. Fig 1 is a schematic representation of one of these 3-state drivers.

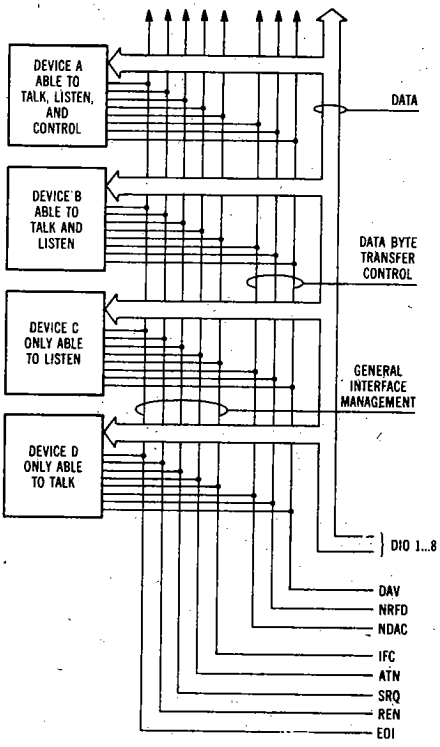
Additional logic was added for decoding the transmit/receive mode control of each of the transceivers. The 8293 was conceived as operating in four distinct modes: talker/listener control transceiver, talker/listener/controller control transceiver, talker/listener data transceiver, and/or talker/listener/controller data transceiver. Thus, a 2-pin select scheme allows a user to select the desired operating mode.

### Choosing appropriate active devices

All of the 8293's functional elements required only four different types of active field effect transistors (FETs). Low threshold enhancement type devices show good high output voltage characteristics, and were used as output pullup devices in push-pull 3-state drivers. Enhancement type FETs were also used for fast switching and low leakage: depletion type devices were used for resistive pullup in buffering. Depletion type FETs also played an important role in meeting the hysteresis specifications of the IEEE 488 standard. Finally, higher threshold depletion type devices were used to prevent the bus lines from being disturbed on power-up and power-down.

A conventional MOS transistor capable of supplying 48 mA at 0.5 V would have been physically too large. HMOS technology, however, permits such a device to be fabricated in an area of less than 150 mil$^2$ (97 mm$^2$). Furthermore, the low speed/power product of HMOS allowed a multi-stage design so that, like transistor-transistor logic (TTL) circuitry, natural hysteresis could be built into the receivers.

**IEEE 488 interface standard**




The IEEE 488 interface standard specifies an 8-bit parallel, bidirectional data bus with eight additional lines for data-byte transfer control and general interface management. The three data-byte transfer lines are data valid (DAV), not ready for data (NRFD), and not data accepted (NDAC). States of these three lines determine when data on the 8-bit data bus are valid, ready to be received, and received, respectively. General interface mangement lines are interface clear (IFC), attention (ATN), service request (SRQ), remote enable (REN), and end or identify (EOI). These lines are used to clear the bus and establish control, initiate polling, pass control from a controller to another controller or the front panel, and indicate the end of a transfer sequence.

### Special layout techniques

The transceiver was implemented using new layout techniques aimed at reducing the series resistance in the polysilicon gate structures of the large transistors, and routing ac signal paths over metal interconnects in order to reduce capacitance and series resistance. Chip size, 188 x 156 mils (5 x 4 mm), includes a 7-mil (0.2-mm) ground line and two ground pads in order to handle the 432-mA current generated when all drivers are on. Power consumption is 300 mW, typically, with driver or receiver speeds of 20 ns under light loads and speeds of 85 ns under the maximum load of 4500 pF.

### Signaling a new trend?

Until the advent of the 8293, complex MOS chips relied on bipolar drivers to handle the heavy bus loading found in complex systems. The 8293 could point the way to future microprocessors and controllers that include their own MOS drivers. Such a scheme would significantly reduce the time lost by going through external buffers. It would also provide all the other benefits of system integration.

The 8293 is essentially a non inverting buffer chip capable of driving high currents. The 8291A talker/listener chip and 8292 GPIB controller chip are designed to interface with the 8080, 8085, iAPX 86, iAPX 88, and 8048/8051 microprocessors and single-chip microcomputers. However, the 8291A and 8292 cannot electrically drive a standard IEEE 488 bus by themselves. Thus, the 8293 was designed to interface between the GPIB and a single 8291A or a combination of the 8291A and 8292. (See Fig 2.)

The chip is divided into nine distinct transceivers. Each one's characteristics, such as 3-state or open-collector outputs, and transmit or receive modes of operation, are determined by internal logic control. (See Fig 3.) Thus, in mode 0 talker/listener control configuration the attention (ATN) transceiver is forced into an input-only mode with respect to the bus's ATN line. The end or identify ($\overline{EOI}$) transceiver, on the other hand, is either a transmitter or receiver depending on the state of the transmit/receive (T/$\overline{R}$2) line. Its interface to the GPIB is 3-state because of the fixed 5 V logic on the $\overline{EOI}$ transceiver's output control. In mode 1, the talker/listener data configuration, the 8293 is a true transceiver with its operations mode controlled by the state of the T/$\overline{R}$1 line and its output characteristics (3-state or open-collector) determined by the states of the $\overline{ATN}$ and $\overline{EOI}$ lines. (See Fig 3.)

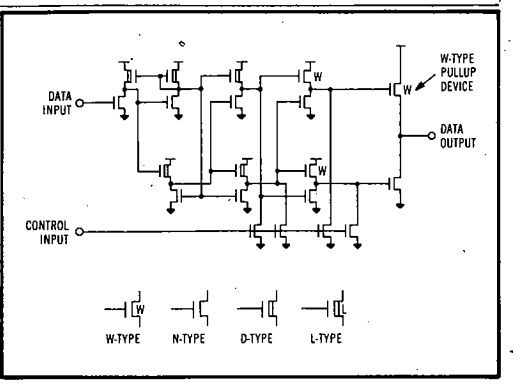



**Fig 1 3-state driver schematic. Nine such open collector drivers are used in the interface.**

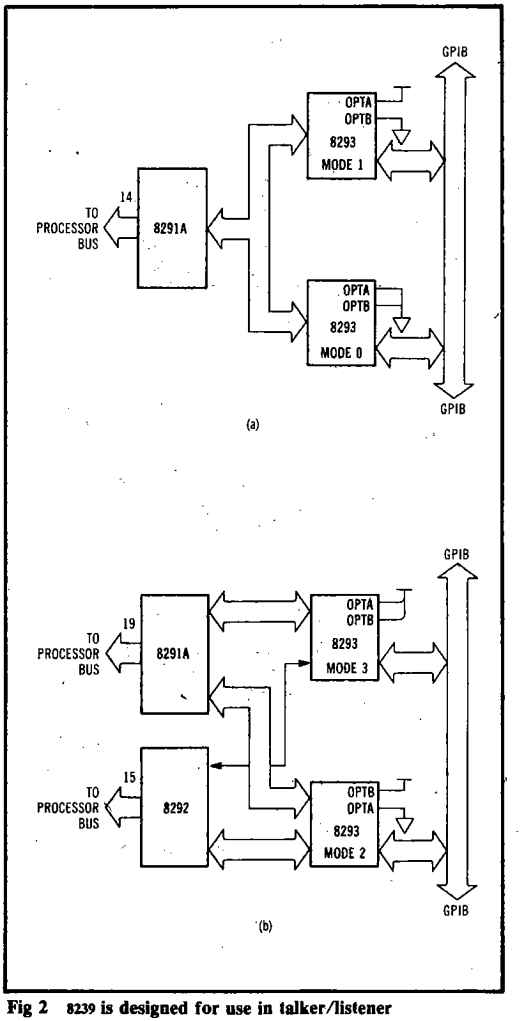



**Fig 2 8239 is designed for use in talker/listener implementation (a), or for talker/listener/controller interface (b).**

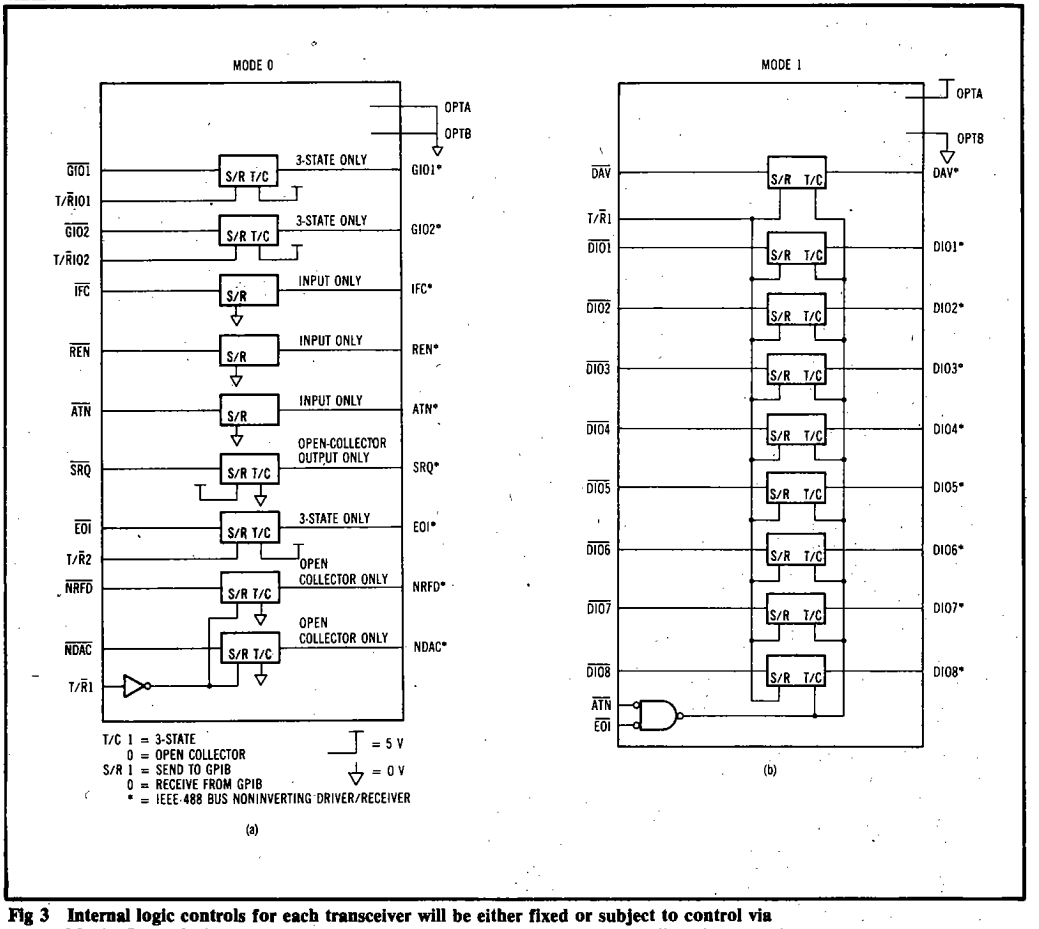



**Fig 3 Internal logic controls for each transceiver will be either fixed or subject to control via external logic. In mode 0, chip is set up for control, thus some transceivers are fixed in transmit or receive mode only. In mode 1, chip is configured as true transceiver—all nine transceivers can transmit or receive depending on state of T/R̄1 pin. In (a) is talker/listener control configuration, and in (b), talker/listener data configuration.**

The talker/listener/controller control configuration, mode 2, is a full transceiver mode but the operation mode of the transceivers is determined by more complex combinational logic. (See Fig 4.) The fourth mode (mode 3), which is the talker/listener/controller data configuration, is again a true transceiver whose mode of operation is controlled by the state of the T/R̄1 line. In this mode, some additional interval combinational logic is enabled to permit the 8293 to support the 8292 in taking bus control synchronously.

***...complete talker/listener/controller mode logic resides in four LSI chips.***

The 8293's overall mode (mode 0, 1, 2, or 3) is determined by the state on the option pins 26 and 27. For example, if both pins are tied low (0 V), the chip is in mode 0. If both are high (5 V) it is in mode 3. The particular state of these pins will determine the characteristics of the other 26 pins. (See the Table, "8293 Mode Selection Pin Mapping.")

### Talker/listener only

If the IEEE 488 is to be implemented in a system that is able to talk and listen (eg, a digital multimeter), only talk (eg, a counter), or only listen (eg, a signal generator),

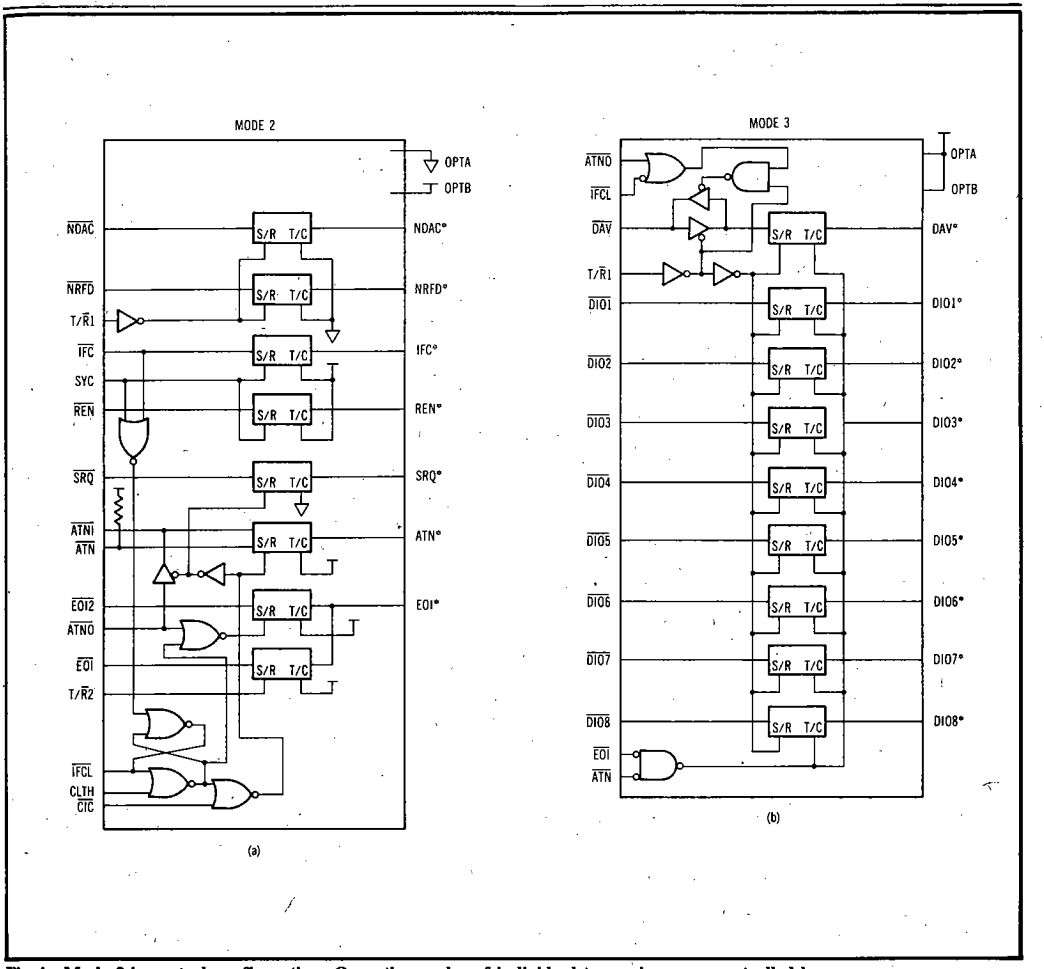



**Fig 4 Mode 2 is control configuration. Operating nodes of individual transceivers are controlled by external signals and internal combinational logic. Chip in mode 3 acts like true transceiver, as in mode 1, except some extra functions have been included in order to support controller function. In (a), talker/listener/controller configuration is for control, and in (b), for data.**

then the entire interface can be built with a single 8291A and a pair of 8293s. (See Fig 5.) In this configuration, one 8293 handles the eight data lines DI01 to DI08 and the other handles the data-byte transfer handshake lines and general interface management lines. Both transceivers are connected to the 8291A's $\overline{ATN}$, and $\overline{EOI}$, and T/$\overline{R1}$ lines.

### Talker/listener/controller

For an IEEE 488 controller (like the HP 85 or Tektronix 4051), the system must be able to take control of the bus or delegate it to another controller. Such an interface scheme can be implemented using an 8291A, an 8292, and a pair of 8293s. (See Fig 6.) The arrangement is similar to that of a talker/listener interface; one 8293 handles the DI01 through DI08 bus data lines and the other handles the data byte transfer handshake and general interface management lines. The difference is that pins 26 and 27 have been selected for modes 2 and 3 and several additional control functions have been added. The attention in (ATNI) lines and attention out (ATNO) lines permit the 8292 to monitor the GPIB's ATN line and take control of the bus. In conjunction with the ATN line, the EOI2 line is used by the 8292 to initiate a polling sequence.

*The chip is divided into nine distinct transceivers and each one's characteristics are determined by internal logic.*

Lastly, the system controller line (SYC) enables the control function. If it is low, the 8292 is prevented from acting as a controller. If it is switched high, the 8292 can act as a controller. In essence, the SYC controls the direction of the interface clear (IFC) and remote enable (REN) signals.

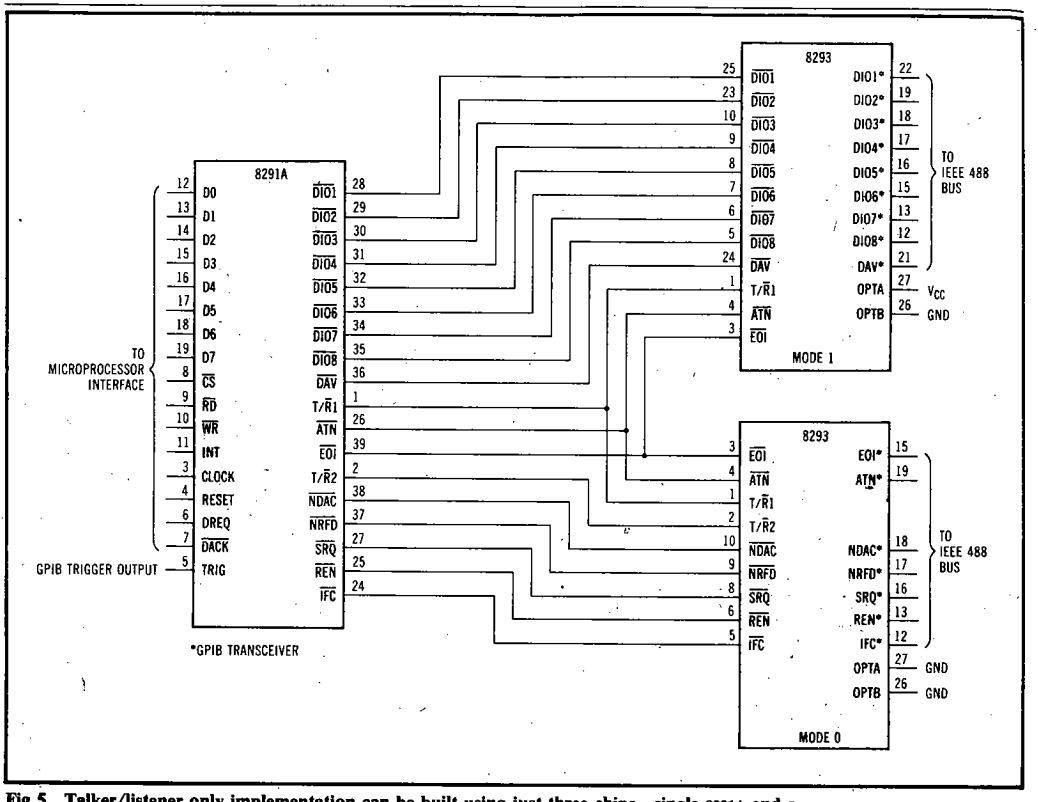
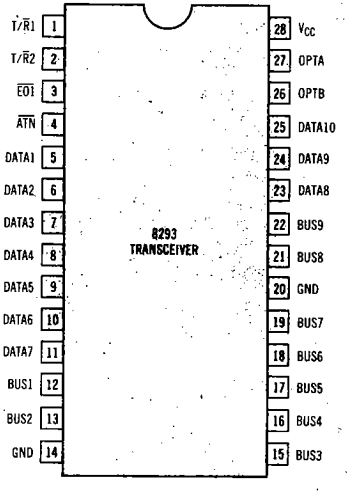



**Fig 5 Talker/listener only implementation can be built using just three chips—single 8291A and a pair of 8293s. First (upper) transceiver chip is used for bidirectional data flow on DIO1 to DIO8 data lines. Lower 8293 handles some of data byte transfer control lines and general interface management lines.**

8293 MODE SELECTION PIN MAPPING

| PIN NAME | PIN NO | IEEE IMPLEMENTATION NAME | | | |
|---|---|---|---|---|---|
| | | MODE 0 | MODE 1 | MODE 2 | MODE 3 |
| OPTA | 27 | 0 | 1 | 0 | 1 |
| OPTB | 26 | 0 | 0 | 1 | 1 |
| DATA1 | 5 | $\overline{IFC}$ | $\overline{DIO8}$ | $\overline{IFC}$ | $\overline{DIO8}$ |
| BUS1 | 12 | IFC* | DIO8* | IFC* | DIO8* |
| DATA2 | 6 | $\overline{REN}$ | $\overline{DIO7}$ | $\overline{REN}$ | $\overline{DIO7}$ |
| BUS2 | 13 | REN* | DIO7* | REN* | DIO7* |
| DATA3 | 7 | NC | $\overline{DIO6}$ | $\overline{EOI2}$ | $\overline{DIO6}$ |
| BUS3 | 15 | EOI* | DIO6* | EOI* | DIO6* |
| DATA4 | 8 | $\overline{SRQ}$ | $\overline{DIO5}$ | $\overline{SRQ}$ | $\overline{DIO5}$ |
| BUS4 | 16 | SRQ* | DIO5* | SRQ* | DIO5* |
| DATA5 | 9 | $\overline{NRFD}$ | $\overline{DIO4}$ | $\overline{NRFD}$ | $\overline{DIO4}$ |
| BUS5 | 17 | NRFD* | DIO4* | NRFD* | DIO4* |
| DATA6 | 10 | $\overline{NDAC}$ | $\overline{DIO3}$ | $\overline{NDAC}$ | $\overline{DIO3}$ |
| BUS6 | 18 | NDAC* | DIO3* | NDAC* | DIO3* |
| DATA7 | 11 | T/R1O1 | NC | ATN1 | ATN0 |
| DATA8 | 23 | T/R1O2 | $\overline{DIO2}$ | ATN0 | $\overline{DIO2}$ |
| BUS7 | 19 | ATN* | DIO2* | ATN* | DIO2* |
| DATA9 | 24 | $\overline{GIO1}$ | $\overline{DAV}$ | $\overline{CIC}$ | $\overline{DAV}$ |
| BUS8 | 21 | GIO1* | DAV* | CLTH | DAV* |
| DATA10 | 25 | GIO2 | DIO1 | IFCL | DIO1 |
| BUS9 | 22 | GIO2* | DIO1* | SYC | DIO1* |
| T/R1 | 1 | T/R1 | T/R1 | T/R1 | T/R1 |
| T/R2 | 2 | T/R2 | NC | T/R2 | IFCL |
| EOI | 3 | $\overline{EOI}$ | $\overline{EOI}$ | $\overline{EOI}$ | $\overline{EOI}$ |
| ATN | 4 | $\overline{ATN}$ | $\overline{ATN}$ | $\overline{ATN}$ | $\overline{ATN}$ |

*These pins are the IEEE 488 bus noninverting driver/receivers. They include all the bus terminations required by the standard, and connect directly to the GPIB connector.



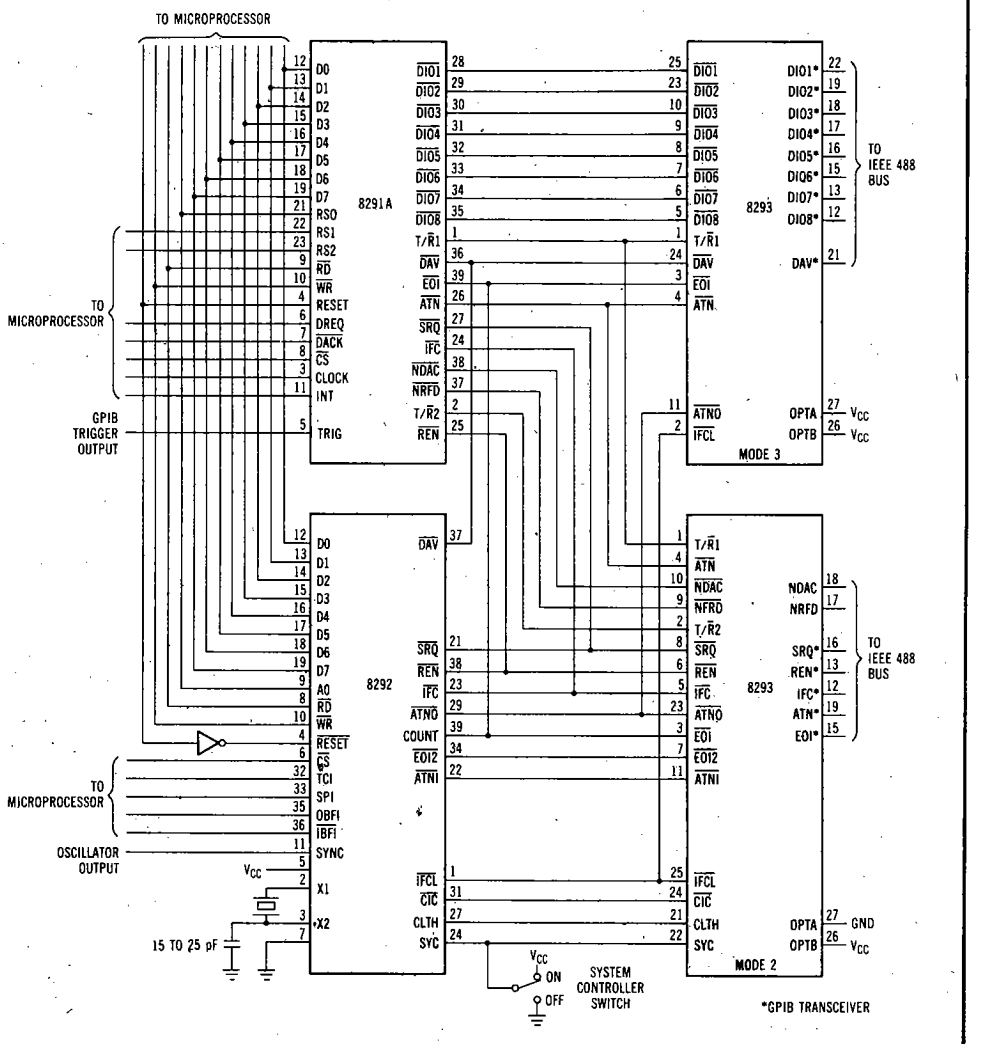



**Fig 6 Fully functional talker/listener/controller interface can be built with only four LSI chips; the 8291A, 8292, and a pair of 8293s. Like simpler talker/listener only case, one 8293 handles data transceiver functions while other handles data byte transfer control and general interface management. There are additional control lines enabled which support the controller (8292) activity.**

## Summary

Before the advent of integrated solutions for IEEE 488 implementation, it usually took forty to fifty SSI and MSI chips to build this interface. A large portion of those were eliminated by controllers and interface chips like the 8291A and 8292. Now, with the last part of the interface available in LSI, a fully functional interface can be built using only four LSI chips. The cost of the original design was typically $400 to $500. A set of the three chips, the 8291A, and two 8293s (for a talker/listener function) allows a 15-fold reduction in cost. The power dissipation of a 40-chip interface was in the vicinity of 10 W. The power dissipation of the 4-chip approach is a mere 1.5 W. The size of the PC board is considerably smaller, too, and that lowers the manufacturing costs and improves reliability.